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EXAMINER	
TRUONG, LECHI	

ART UNIT	PAPER NUMBER
2194	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/517,236	VAZEILLE ET AL.	
	Examiner	Art Unit	
	LECHI TRUONG	2194	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 December 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-14 and 16-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1, 3-14, 16-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1, 3-14, 16-26 are presented for the examination. Claims 2, 15 are cancelled.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 3-6, 8, 9, 11, 18, 20, 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Suzuki et al. (U. S. patent application publication no. 2003/0046324) hereinafter referenced as Suzuki, in view of Jamadagni et al. (U. S. patent application publication no 20020152185), hereinafter referenced as Jamadagni in view of Henning (US 4538235 A) and further in view of Nakamura (US 5748967 A).

3. **As to claim 1**, Suzuki discloses a method of managing events ("*tasks*" *with* "*information obtained from the target to be monitorially controlled", or "information obtained from the network communication system",* disclosed at page 6, paragraph 0125) in a standard computer system comprising a central unit ("*CPU*") connected to memory units (*memory for*

"communication task group", "control task group", and "management task group", disclosed at page 1, paragraph 0013) and peripheral devices *("devices" connected to an "I/O interface"*, disclosed at page 4, paragraph 0078) by a data bus ("*bus*") allowing a multi-master configuration ("*...in accordance with the invention, there is provided a distributed control system, comprising a plurality of any of the above-described controllers. In this case, the controllers are disposed in a distributed manner*", as disclosed at paragraph 0031 and figure 43). The method comprising the following steps: receiving events *("...information obtained from the target to be monitorially controlled or the network communication system is processed*", disclosed at page 1, paragraph 0012*)*, storing the events *(...managing the plurality of tasks stored in the memory*", paragraph 0013), assigning at least one appropriate action to each received event, and executing that action in response to the received event *("...a program including an operating system for controlling the execution of the tasks, wherein the plurality of tasks are managed by being classified into a communication task group for performing communications with a network communication system, and a control task group for monitorially controlling a target to be monitorially controlled"*, paragraph 0012), which method is characterized in that the above-mentioned management steps are carried out in real time *("...objects of the present invention are to provide a controller capable of guaranteeing both real-time execution of control processing and throughput of network communication processing by one information processing means"*, paragraph 0011).

4. However, Suzuki fails to disclose that the events are time-stamped. However, the examiner maintains that it was well known in the art that there is an event processing system that time-stamp the event, as taught by Jamadagni.

5. In the similar field of endeavor, Jamadagni disclosed the following: *"...a raw event consists of a time stamp, the event type, event subtype, equipment ID, severity of the event, description, etc."* as disclosed at page 4, paragraph 0064.

6. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Suzuki by adding the receiving time-stamp for the "*information obtained from the target to be monitorially controlled*" or "*information obtained from the network communication system*" that associated with the task, as taught by Jamadagni. This modification allows Suzuki invention to capture the time the event is received.

7. Suzuki and Jamadagni do not teach steps carry out in real time without access to the central unit by a management unit included in an independent management module connected to the data bus and incorporated into the standard computer system. However, Henning teaches steps carry out in real time without access to the central unit by a management unit included in an independent management module connected to the data bus and incorporated into the standard computer system (Outputs of the control register are connected to the microcomputer data bus so that the processor may read the contents of the control register at any time. The use of controlled latch and counter register for the interval counter circuitry allows the detection of intervals to be performed without requiring the processor to execute instructions to monitor the input signal status after each clock pulse. The counter register is automatically reloaded from the latch after each input signal transition so that the interval counter may be retriggered without requiring acting by the processor. Therefore, the construction allows detection of time intervals between input signals without requiring undue amounts of attention from the processor. The interval counter circuitry operates independently of the microcomputer processor in order to measure the

time duration between events by counting clock signals in a decrementing counter and in order to automatically reset its counter as each input signal is received, col 3, ln 1-16).

8. It would have been obvious to one of the ordinary skill in the art at the time the invention was made to modify the teaching of Suzuki and Jamadagni with Henning to incorporate the feature of steps carry out in real time without access to the central unit by a management unit included in an independent management module connected to the data bus and incorporated into the standard computer system because this allows computer processor control over the detection of external events, prior interval counter circuitry has been inadequate to provide the needed performance.

9. Suzuki and Jamadagni and Henning do not teach Nakamuro teaches storing each event in a first memory and a second memory and the first memory and the second memory are associated with the management unit, the first memory storing events to be processed by the independent management module and the second memory storing events so that these events may be read via the data bus. However, Nakamuro teaches storing each event in a first memory and a second memory and the first memory and the second memory are associated with the management unit, the first memory storing events to be processed by the independent management module and the second memory storing events so that these events may be read via the data bus(a first microprocessor system including a first microprocessor, a first rewritable memory for storing a program and a first system bus connected to said first microprocessor and said first rewritable memory, said first microprocessor reading out the program stored in said first rewritable memory through said first system bus to execute the program read out; a second microprocessor system including a second microprocessor, a second rewritable memory for

storing a program and a second system bus connected to said second microprocessor and said second rewritable memory, said second system bus being separate from said first system bus, and said second microprocessor reading out the program stored in said second rewritable memory through said second system bus to execute the program read out from said second rewritable memory, independently of execution by said first microprocessor, releasing said second system bus by said second microprocessor, in response to a request from said first microprocessor, col 7, ln 50-67 to col 8, ln 1-5).

10. It would have been obvious to one of the ordinary skill in the art at the time the invention was made to modify the teaching of Suzuki , Jamadagni and Henning with Nakamuro to incorporate the feature of storing each event in a first memory and a second memory and the first memory and the second memory are associated with the management unit, the first memory storing events to be processed by the independent management module and the second memory storing events so that these events may be read via the data bus because this guarantees reliability of operation of the microprocessor, the number of ROM change operations is disadvantageously limited.

11. **As to claim 3**, Suzuki and Jamadagni discloses everything as in claim 1 rejection. It is also well known in the art that the times scale for real-time system can be adjusted down to a desired level that enable a system to work efficiently.

12. **As to claim 4**, Suzuki and Jamadagni discloses everything as in claim 1 rejection. However, Suzuki fails to disclose that the independent management module (*the controller*) is isolated from the central unit (*other controllers or personal computers in the network*) by a bridge. However, the examiner maintains that it was well known in the art that there is an event

processing system that uses bridges to filter data in a network, as taught by Jamadagni. In the similar field of endeavor, Jamadagni disclosed a bridge in (disclosed in figure 8) that filter incoming data from the rest of the network.

13. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Suzuki by adding a bridge between the Network control Circuit and the LAN, as taught by Jamadagni. This modification allows Suzuki's network to minimize noise by filters data traffic at the network boundary.

14. **As to claim 5**, Suzuki and Jamadagni disclose everything as in claim 1 rejection. Suzuki also discloses that action (task) is read in a table of actions ("task Control Table", disclosed at page 5, paragraph 104; and figure 5) associated with the management unit (controller) and is preprogrammed via the data bus (Suzuki's invention is a programmable controller with task Control Table stored in memory. The memory is connected to the Network Control Circuit via a bus. It is inherent that the preprogrammed task control table must be transmitted through the bus).

15. **As to claim 6**, Suzuki and Jamadagni discloses everything as in claim 1 rejection. Suzuki and Jamadagni also discloses that events (*tasks*) received by the management unit (*Controller*) are time-stamped to accuracy of the order of 100 nanoseconds (see claim 3 rejection) and stored in a second memory (*"...managing the plurality of tasks stored in the memory by classifying them into a communication task group for performing network communications and a control task group for monitorially controlling the target to be monitorially controlled*", disclosed at page 1, paragraph 0013) associated with the management unit ("controller") so that these events may be read via the data bus in order to store and monitor

these events (The CPU, the memory, the I/O interface, and the network control circuit are connected via the bus, disclosed at figure 1).

16. **As to claim 8**, Suzuki and Jamadagni discloses everything as in claim 1 rejection. Suzuki also discloses that events received by the management unit come from a unit adjacent the management module (disclosed in figure 43).

17. **As to claim 9**, Suzuki and Jamadagni discloses everything as in claim 1 rejection. Suzuki also discloses that events received by the management unit come from equipment external to the computer system (disclosed in figure 43).

18. **As to claim 11**, it is rejected for the same reason as claim 4 (using bridges to filter data).

19. **As to claim 18** is rejected for the same reason as claim 3 – 6.

20. **As to claim 20,** is rejected for the same reason as claim 8.

21. **As to claim 21** is rejected for the same reason as claim 9.

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22. **Claims 7** and **19** are rejected under 35 U.S.C. 103(a) as being unpatentable over Suzuki et al. (U. S. patent application publication no. 2003/0046324) hereinafter referenced as Suzuki, and Jamadagni et al. (U. S. patent application publication no 20020152185), hereinafter referenced as Jamadagni in view of Henning (US 4538235 A) and in view of Nakamura(US 5748967 A) in view of Collins et al. (U. S. patent application publication no 2003/0197632), hereinafter referenced as Collins.

23. **As to claim 7**, Suzuki , Jamadagni and Henning disclose everything as in claim 1 rejection. However, Suzuki fails to disclose that events received by the management unit are

generated by a clock register internal to the management. However, the examiner maintains that it was well known in the art that there is an event processing system that uses clock to generate events, as taught by Collins. In the similar field of endeavor, Collins disclosed a clock control event generated by the event processor (disclosed in figure 1).

24. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Suzuki by adding a clock control event inside the controller, as taught by Collins. This modification allows Suzuki's invention to generate internal invents or signals that are controlled by a clock.

25. **As to claim 19** is rejected for the same reason as claim 7.

26. **Claims 10, 13, 17, 22 - 23** are rejected under 35 U.S.C. 103(a) as being unpatentable over Suzuki et al. (U. S. patent application publication no. 2003/0046324) hereinafter referenced as Suzuki, and Jamadagni et al. (U. S. patent application publication no 20020152185), hereinafter referenced as Jamadagni in view of Henning (US 4538235 A) and further in view of Nakamura(US 5748967 A) and further in view of Rubin et al. (U. S. patent application publication no 2003/0197632), hereinafter referenced as Rubin.

27. **As to claim 10**, Suzuki , Jamadagni and Henning disclose everything as in claim 8 rejections. However, Suzuki fails to disclose that events received by the management unit are synchronized to a frequency corresponding to that of a clock internal to the computer system, as taught by Rubin. In the similar field of endeavor, Rubin disclosed an integrated digital controller comprises at least one digital phase locked loop for synchronizing a module selected from the

group consisting of the pulse sequence generator (PSG) module and the loop control module to the external event, as disclosed at page 3, paragraph 0033.

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28. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Suzuki by adding a digital phase locked loop inside the controller (I/O interface and Network control circuit), as taught by Rubin. This modification allows Suzuki's invention to efficiently process invent signals coming from the external devices and the network.

29. **As to claims 22 , 23** are rejected for the same reason as claim 10.

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30. **As to** claims **13 & 17**, Suzuki, Jamadagni and Henning disclose everything as in claim 1 rejection. However, Suzuki fails to disclose that the memory is the **random- access memory (RAM),** and the **RAM is the double-port type**. However, the examiner maintains that it was well known in the art that there is an event processing system that uses the double-port RAM, as taught by Rubin. In the similar field of endeavor, Rubin disclosed integrated digital controller comprises the ADC Scanner where the Scanning engine is a memory-based unit that uses an over-sampling method, thus the required signals are stored in a RAM (disclosed at page 5, paragraph 0066) and Preferably, memory is a dual port RAM (disclosed at page 15, paragraph 0182).

31. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Suzuki by upgrade the memory unit with double-port RAM inside the controller, as taught by Rubin. This modification allows Suzuki's invention to facilitate the task control table update. The double port RAM also allows the memory read and writes to be independent from one another (faster memory access).

32. As to claims **12** and **24** are rejected under 35 U.S.C. 103(a) as being unpatentable over Suzuki et al. (U. S. patent application publication no. 2003/0046324) hereinafter referenced as Suzuki, and Jamadagni et al. (U. S. patent application publication no 20020152185), hereinafter referenced as Jamadagni in view of Henning (US 4538235 A) in view of Nakamura (US 5748967 A) and further in view of David R. Cheriton (U. S. patent no 5,893,155), hereinafter referenced as Cheriton.

33. **As to claim 12**, Suzuki and Jamadagni disclose everything as in claim 1 rejection. However, Suzuki fails to disclose that the management unit generates an interrupt if it is not possible to associate an event with an action, as taught by Cheriton.

34. In the similar field of endeavor, Cheriton disclosed a digital computer memory cache organization for efficient data logging. It comprises a control module that accesses a log translation table and select the log translation entry (disclosed at page 17, line 65-68), When a translation is missing, the system generates an interrupt that is handled by operating system software (disclosed at page 19, line 33 – 35).

35. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Suzuki by adding the interrupt process when the signal does not match any action stored in the memory, as taught by Cheriton. This modification allows Suzuki's invention to identify invalid inputs coming from the network or from other external devices.

36. **As to claim 24** is rejected for the same reason as claim 11 and 12.

37. **Claim 14** is rejected under 35 U.S.C. 103(a) as being unpatentable over Suzuki et al. (U. S. patent application publication no. 2003/0046324) hereinafter referenced as Suzuki, and Jamadagni et al. (U. S. patent application publication no 20020152185), hereinafter referenced as Jamadagni in view of Henning (US 4538235 A) and further in view of Nakamura (US 5748967 A) view of Rubin et al. (U. S. patent application publication no 2003/0197632) and further in view of Sven et al. (U. S. patent application publication no. 2003/0005099), hereinafter referenced as Sven.

38. **As to claim 14,** Suzuki, Jamadagni and Henning, Nakamura disclose everything as in claim 13 rejections. However, Suzuki fails to disclose that the data bus is a standard bus selected from the group comprising a PCI bus, a VME bus, a compact PCI bus and a USB bus, as taught by Sven.

39. In the similar field of endeavor, Sven disclosed a control management system that has input devices and processing unit connected to a system bus or a universal serial Bus (USB) (disclosed at page 3, paragraph 0026).

40. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Suzuki by substituting the "bus" with the USB bus, as taught by Sven. This modification allows Suzuki's invention to have many peripherals to be connected using a single standardized interface.

41. **Claims 16** and **25** are rejected under 35 U.S.C. 103(a) as being unpatentable over Suzuki et al. (U. S. patent application publication no. 2003/0046324) hereinafter referenced as Suzuki in view of Jamadagni et al. (U. S. patent application publication no 20020152185), hereinafter referenced as Jamadagni in view of Henning (US 4538235 A) in view of Nakamura (US 5748967 A) in view of Rubin et al. (U. S. patent application publication no 2003/0197632) in view of Sechi et al. (U. S. patent no. 6,639,538), hereinafter referenced as Sechi.

42. **As to claim 16**, Suzuki, Jamadagni and Henning disclose everything as in claim 13 rejections. However, Suzuki fails to disclose that the first memory and the second memory (*memory for "communication task group", "control task group", and "management task group")* are of the FIFO type.

43. However, the examiner maintains that it was well known in the art that there is a system that uses FIFO type memory, as taught by Sechi.

44. In the similar field of endeavor, Sechi disclosed a monitoring system that has the memory buffer operates in FIFO (first-in, first-out) fashion; that is, digital data samples exit the memory buffer in the order that the digital data samples arrive at the memory buffer (disclosed at page 9, line 66 and 67).

465 Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Suzuki by substituting the memory with the FIFO type memory, as taught by Sechi. This modification allows Suzuki's invention to allow incoming task event) to be executed sequentially, in a pipelined manner.

46. **As to claim 25** are rejected for the same reason as claims 15 and 16.

47. **Claim 26 is** rejected under 35 U.S.C. 103(a) as being unpatentable over Suzuki et al. (U. S. patent application publication no. 2003/0046324) hereinafter referenced as Suzuki, and Jamadagni et al. (U. S. patent application publication no 20020152185), hereinafter referenced as Jamadagni in view of Henning (US 4538235 A) and further in view of Nakamura(US 5748967 A) in view of Rubin et al. (U. S. patent application publication no 2003/0197632), hereinafter referenced as Rubin and further in view of Iwasa(US 5522058 A).

48. **As to claim 26**, Suzuki, Jamadagni, Henning, Nakamura, Rubin do not explictlly teach the first memory and the second memory are internal to the management unit. However, Iwasa teaches the first memory and the second memory are internal to the management unit(each processor unit comprising: a central processing unit (CPU); a main memory connected with the CPU through an internal bus, for storing a distributed part of data entries of a shared-memory of the system; a cache memory associated with the CPU and connected with the main memory through the internal bus, for caching selected data entries of the shared-memory, col 3, ln 5-20).

49. It would have been obvious to one of the ordinary skill in the art at the time the invention was made to modify the teaching of uzuki, Jamadagni, Henning, Nakamura, Rubin with Iwasa to incorporate the feature ofst memory and the second memory are internal to the management unit because this allows the consistency among the memories can be maintained without unnecessarily increasing the traffic on the shared bus.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to LeChi Truong whose telephone number is (571) 272-3767. The examiner can normally be reached on 8 - 5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sough Hyung can be reached on (571) 272-6799. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR of Public PAIP. Status information for unpublished

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system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIP

system, contact the Electronic Business Center (EBC) at 866-217-9197(toll-free).

/LeChi Truong/
Primary Examiner, Art Unit 2194